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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/757,491	01/11/2001	Haruo Tanaka	P107400-00021	8241
7590	02/07/2005		EXAMINER	
ARENT FOX KINTNER PLOTKIN & KAHN PLLC 1050 Connecticut Avenue, N.W., Suite 600 Washington, DC 20036-5339			NGUYEN, JENNIFER T	
			ART UNIT	PAPER NUMBER
			2674	

DATE MAILED: 02/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>
	09/757,491	TANAKA ET AL.
	<b>Examiner</b>	<b>Art Unit</b>
	Jennifer T Nguyen	2674

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

1)  Responsive to communication(s) filed on 11 January 2001.

2a)  This action is **FINAL**.                            2b)  This action is non-final.

3)  Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

4)  Claim(s) 2-9 and 11 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5)  Claim(s) \_\_\_\_\_ is/are allowed.

6)  Claim(s) 2-9 and 11 is/are rejected.

7)  Claim(s) \_\_\_\_\_ is/are objected to.

8)  Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

9)  The specification is objected to by the Examiner.

10)  The drawing(s) filed on \_\_\_\_\_ is/are: a)  accepted or b)  objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)  The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)  Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a)  All b)  Some \* c)  None of:  
1.  Certified copies of the priority documents have been received.  
2.  Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3.  Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1)  Notice of References Cited (PTO-892)  
2)  Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3)  Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.

4)  Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.  
5)  Notice of Informal Patent Application (PTO-152)  
6)  Other: \_\_\_\_\_.

## **DETAILED ACTION**

1. This Office action is responsive to amendment filed on 08/09/2004.
2. Claims 5 and 6 are objected to because of the following informalities: the phrase “an MFS structure or an MFIS structure” in claim 5 and the phrase “an MFMIS structure” in claim 6 are not clear, please spell out.

### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 2-8 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. (Patent No. US 5,349,366) in view of Black et al. (Patent No. US 6,069,381).

Regarding claim 2, referring to Fig. 1A, Yamazaki teaches a display device comprising: a display element (LC); a control element (Tr2) for controlling a voltage to be applied to the display element to drive the display element; and a nonvolatile data holding section (FE) connected to said control element wherein the control element (Tr2) is formed of MOS transistor type element (i.e., NMOS type), one of a drain and a source of the MOS transistor type element is connected to the display element and the other is connected to a driving line (Vlc), a gate side of the MOS transistor type element is connected to a control line (Vd) through the nonvolatile data holding section (FE), and plural sets of the display element (LC), the control element (Tr2) and the nonvolatile data holding section (FE) are formed as each pixel in a matrix (col. 10, lines 21-46).

Yamazaki differs from claim 2 in that he does not specifically teach the nonvolatile data holding section capable of holding control data of said control element in a floating state. However, Black teaches a nonvolatile data holding section capable of holding control data of said control element in a floating state (col. 4, lines 25-67). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate the nonvolatile data holding section capable of holding control data of said control element in a floating state as taught by Black in the system of Yamazaki in order to provide a data holding memory section which can be read and written using low voltages.

Regarding claim 3, Yamazaki teaches a selective transistor (Tr1) is connected between said nonvolatile data holding section (FE) and said control line (Vd), and a gate of said selective transistor is connected to a selective line (Vg) (Fig. 1A).

Regarding claim 4, Yamazaki teaches the nonvolatile data holding section is formed of a ferroelectrics capacitor (col. 10, lines 21-29).

Regarding claim 5, the combination of Yamazaki and Black teaches the control element and said nonvolatile data holding section are formed of a transistor having an MFS structure or an MFIS structure in which a ferroelectric capacitor is formed integrally on the gate side of a MOS transistor, a back gate of said MOS transistor is connected to a write line, and the control data can be written to said nonvolatile data holding section between said control line and said write line (Fig. 7, col. 5, line 58 to col. 6, line 13 of Black).

Regarding claim 6, the combination of Yamazaki and Black teaches the control element and said nonvolatile data holding section are formed of a transistor having an MFMIS structure in which a ferroelectric capacitor is connected to the gate side of a MOS transistor through a

common electrode or a wiring, a capacitor is connected between a connecting portion of a gate electrode of said MOS transistor and said ferroelectric capacitor and a ground or a write line, and the control data can be written to said nonvolatile data holding section between said control line and said ground or said write line (Fig. 7, col. 5, line 58 to col. 6, line 13 of Black).

Regarding claim 7, the combination of Yamazaki and Black teaches the nonvolatile data holding section is constituted by an element utilizing a magnetoresistance effect (from col. 5, line 38 to col. 6, line 13 of Black).

Regarding claim 8, the combination of Yamazaki and Black further teaches the nonvolatile data holding section (31) is constituted by a single electron memory (col. 6, lines 1-13 of Black).

Regarding claim 11, Yamazaki teaches the control element is formed of a MOS transistor (Tr2), said nonvolatile data holding section (C3) is formed of a ferroelectric capacitor which is connected to a gate of said MOS transistor type element, and a capacitor (C2) is connected between a connecting portion of said gate with said ferroelectric capacitor and a write line (Vlc), wherein the control data is written to said nonvolatile data holding section by using said control line and said write line (fig. 4A) (col. 15, lines 18-45).

5. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. (Patent No. US 5,349,366) in view of Black et al. (Patent No. US 6,069,381) and further in view of Nakamura (Patent No. US 6,563,480).

Regarding claim 9, the combination of Yamazaki and Black differs from claim 9 in that it does not specifically teach the display element is formed by an organic EL element. Nakamura teaches the display element is formed by an organic EL element (col. 2, lines 12-25). Therefore,

it would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate the display element is formed by an organic EL element as taught by Nakamura in the system of the combination of Yamazaki and Black in order to provide a display panel fabricated at a low cost, having a reduced occupied area and capable of operating at a higher speed.

6. Applicant's arguments with respect to claims 2-9 and 11 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Jennifer T. Nguyen** whose telephone number is **703-305-3225**. The examiner can normally be reached on Mon-Fri from 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Richard A Hjerpe** can be reach at **703-305-4709**.

**Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks

Washington, DC. 20231

**Or faxed to: 703-872-9306 (for Technology Center 2600 only)**

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, sixth-floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding

should be directed to the Technology Center 2600 Customer Service Office whose telephone number is 703-306-0377.

JNguyen  
01/21/2005



REGINA LIANG  
PRIMARY EXAMINER